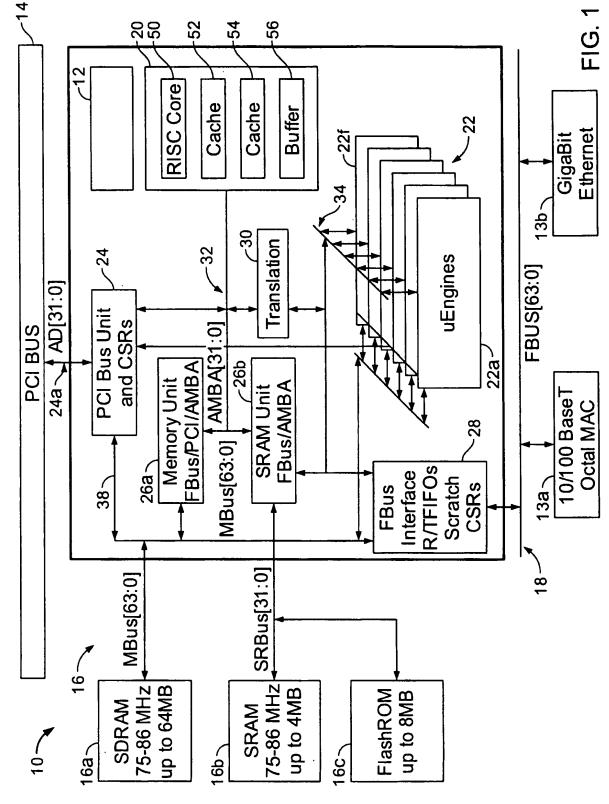
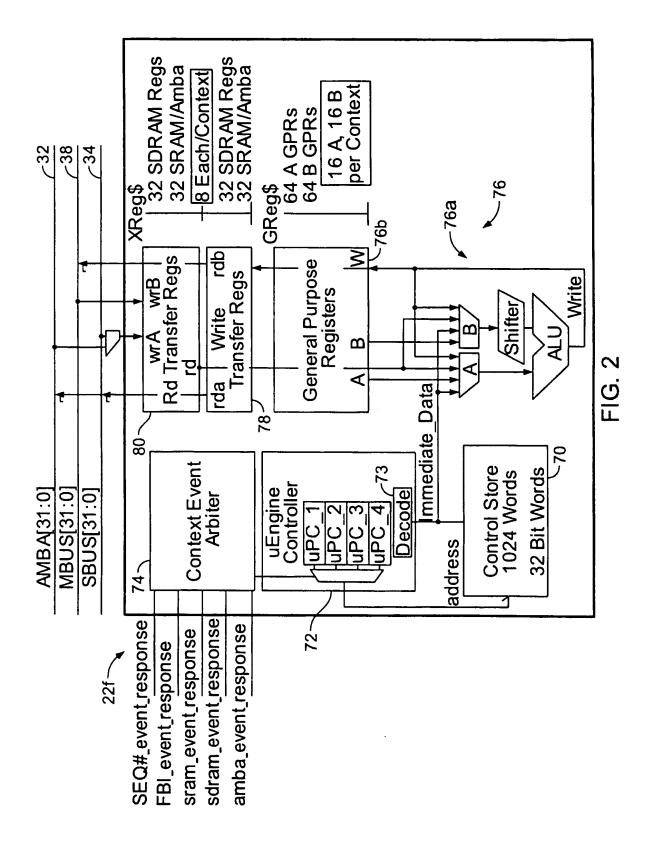
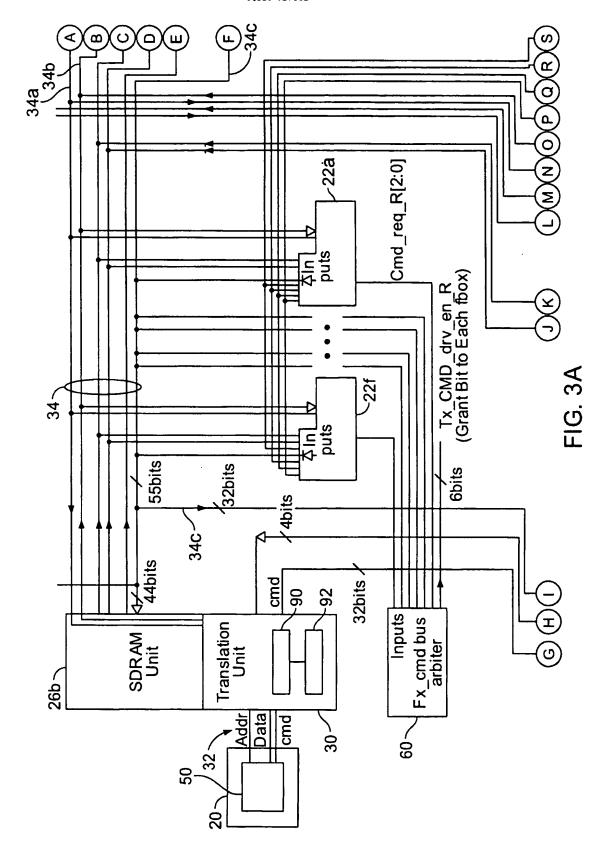


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Sbus_push_addr_R<4:0> & Sbus_push_ld_R<3:0> Sbus_pull_addr_R<4:0> & Sbus_pull_Id_R<3:0> T_cmd_type_R<2:0> (Unit Address) Sram_sdone_Tbox_R<2:0> Sbus_push_data_R<31:0> T_cmd_bus_R<54:0> Sets Sram_sdone_ctx_R<1:0> Sbus_pull_data_R<31:0> 000 none 001 Sram Chain 010 SDR Chain 011 Sram 100 SDR 110 PCI Cmd_Req_R<2:0> (IL $\boldsymbol{\omega}$

PR				
Sram_puXX_addr_R<4:0> [4:0] xfer_reg_addr	Sram_puXX_ID_R<3:0> 0-5 Fboxes 8-13 Fboxes_csr 6 fbi 15 nop			
Sdram_puXX_addr_R<6:0> [4:0] xfer_reg_addr if not TFIFO [6:0] TFIFO_addr	Sdram_puXX_ID_R<3:0> 0-5 Fboxes 8-13 Fboxes_csr 6 fbi 15 nop			

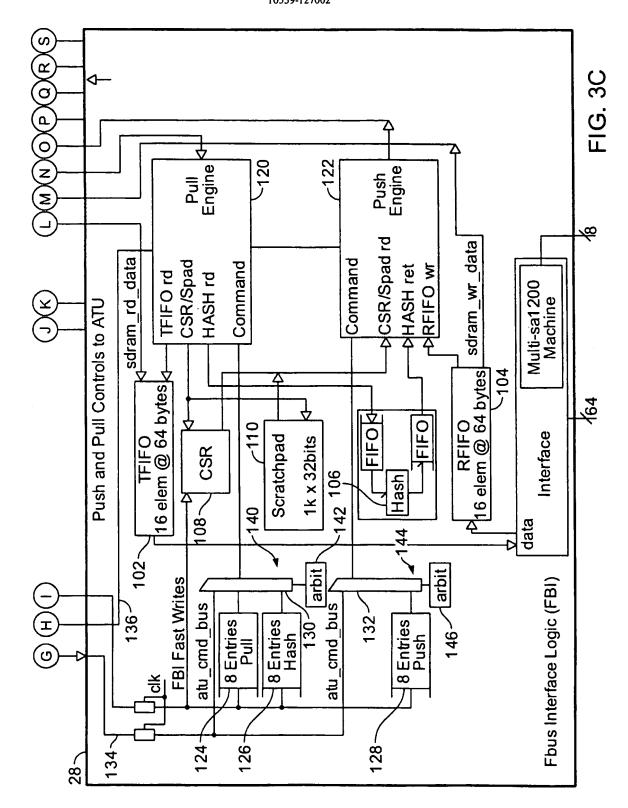
Scratch

Tx_CMD_drv_en_

R<1:0>

0 none 1 grant

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	ESS SPACE DECIMAL)			
FFFF FFFF				
E7FF FFFF	-			
E000 0000	_			
C000 0000	SDRAM	HEXADECIMAL	MAPPED ADDRESSES	XXXX (BINARY)
		B004 XXXX	FBUS INTERFACE (28) SCRATCHPAD (110)	0100 xxxx xxxx xxxx
B000 0000	TRANSLATION UNIT 30	B004 XXXX	FBUS INTERFACE(28) REGISTERS (108)	0000 xxxx xxxx xxxx
A000 0000	PCI CONFIG	B000 XXXX	MICRO-ENGINE (22a) REGISTERS (78, 80)	0110 1xxx xxxx xxxx
9000 0000	SYSTEM	,	MICRO-ENGINE (22b) REGISTERS (78, 80)	0110 0xxx xxxx xxxx
8000 0000	MAC & SRAM CONTROL REGISTERS		MICRO-ENGINE (22c) REGISTERS (78, 80)	0001 1xxx xxxx xxxx
			MICRO-ENGINE (22d) REGISTERS (78, 70)	0001 0xxx xxxx xxxx
4000 0000	PCI UNIT		MICRO-ENGINE (22e) REGISTERS (78, 80)	0000 1xxx xxxx xxxx
			MICRO-ENGINE (22f) REGISTERS (78, 80)	0000 0xxx xxxx xxxx
0000 0000	SRAM			
		B000 XXXX	MICRO-ENGINE (22a) REGISTERS (76b)	0010 1xxx xxxx xxxx
			MICRO-ENGINE (22b) REGISTERS (76b)	1101 0xxx xxxx xxxx
			MICRO-ENGINE (22c) REGISTERS (76b)	0001 1xxx xxxx xxxx
			MICRO-ENGINE (22d) REGISTERS (76b)	0001 0xxx xxxx xxxx
			MICRO-ENGINE (22e) REGISTERS (76b)	0000 1xxx xxxx xxxx
			MICRO-ENGINE (22f) REGISTERS (76b)	0000 0xxx xxxx xxxx

FIG. 4

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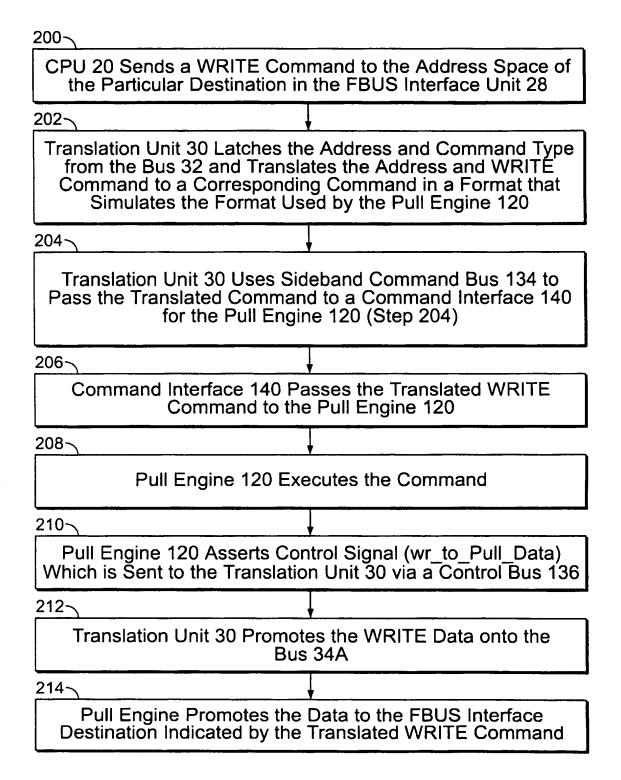
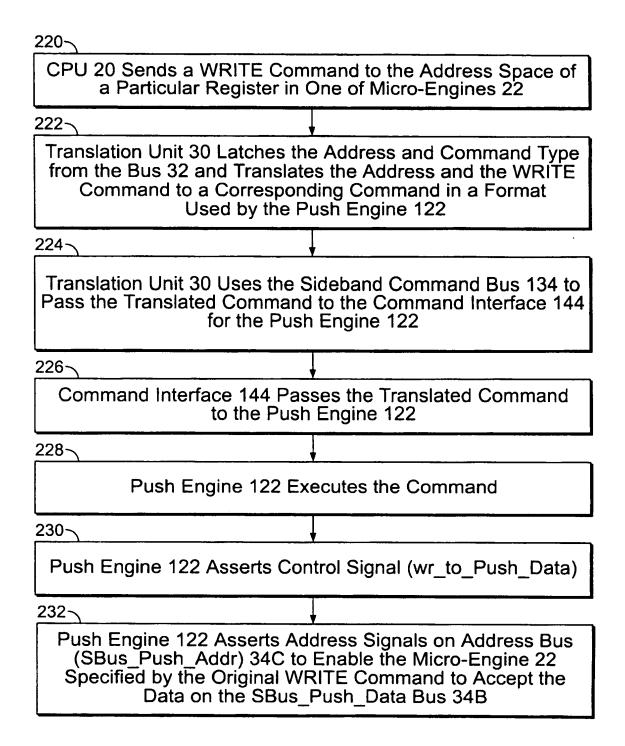
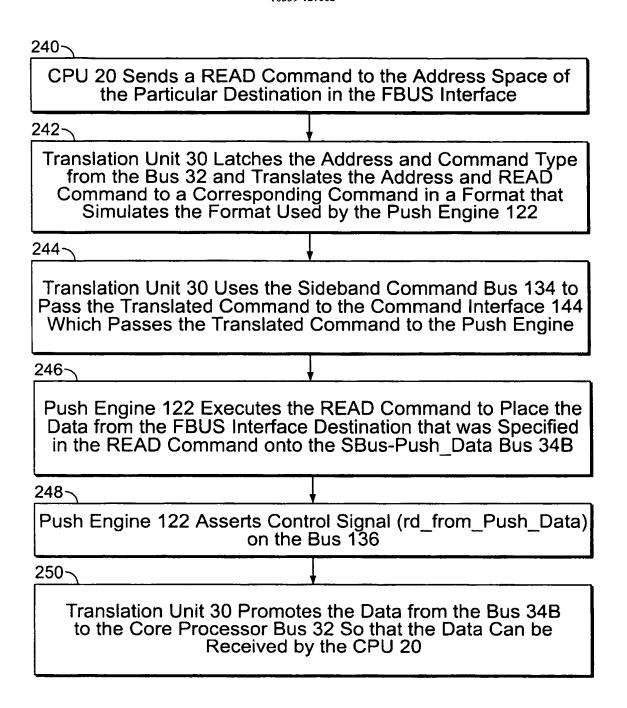


FIG. 5

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